SCSI Passive Interconnect Performance

White Paper Prepared for the SCSI Trade Association

Paul Aloisi, Distinguished Member of the Technical Staff, Texas Instruments
Board Member and Director of SCSI Trade Association

The SCSI Passive Interconnect Performance (PIP) standard establishes the test methods for bulk cables, cable assemblies and backplanes. It provides a method of measuring and validating the passive components in the SCSI system to ensure operation at higher speeds. The SCSI standards in the past have specified only bulk cable rules. There were no rules or guidelines for cable assemblies and backplanes.

SCSI continues to address the issues of a multidrop bus to provide lower cost and higher performance than other interface standards. SCSI has a 16-bit data path that is out performing 32- and 64-bit data path system buses with distances in meters, not inches. Serial buses become parallel serial buses at higher speeds that only work in point-to-point applications requiring switch technology to add devices.

Why Passive Interconnect is Important

The passive interconnect system is becoming more important as speeds increase. Ultra320 and Ultra640 SCSI speeds have a frequency content of 80 and 160 MHz respectively. There are two bytes per transfer and the data is clocked on the rising and falling edge of the clock. The frequency on the bus is a quarter of the transfer speed in bytes. Spacing of connectors at quarter wavelengths produce period structures which form comb filters and create a Bloch impedance that is much lower than the expected system impedance. Bloch impedance can be 30 percent of the transmission line impedance when the reflect wave is exactly out of phase with the next wave. The spacing of the devices or structures is the key factor in comb filters and Bloch impedance. Standard twist and flat spacing becomes a major problem at 160 MHz – the first pole of the comb filter. (See Figure 1 for an example of the comb filter structure using a typical twist and flat cable).

Dielectric material, spacing and impedance are critical at over 100 MHz. The dielectric is the main factor in propagation time and the frequency roll off of the system. Polyvinyl Chloride (PVC) and Fiberglass Printed Circuit board (FR4) roll off is a major issue for intersymbol interference (ISI). Better dielectric material like FEP, TPE and TPO should be used for cables. SCSI is a base band system with frequency content from DC to the maximum frequency. This creates a major problem for isolated ones or zeros which may not reach the zero crossing level on large configurations. The signal may only reach 30 percent of the low frequency amplitude in one-bit time. Ultra320 SCSI requires driver precompensation to reduce the problem – the first bit driven harder than successive bits after a transition.

The driver has a fixed precompensation level. If a system has too much roll off of the driver, precompensation is not adequate for the system to operate. PIP specifies how to test for the roll off allowed in the system. The basic impedance test uses a time domain reflectometer test (TDR) that shows the uniformity of the SCSI bus segment. A swept frequency test is used to catch problems with periodic structures that can create major attenuation problems at the operating frequencies. The swept frequency test uses a vector network analyzer (VNA) to sweep from 300 KHz to 600 MHz. Ultra320 SCSI and beyond run at specific frequencies. Historically, SCSI ran at speeds up to the maximum frequency. Any speeds up to the maximum speed were negotiated. The frequency range made it impossible to specify around periodic structure problems.

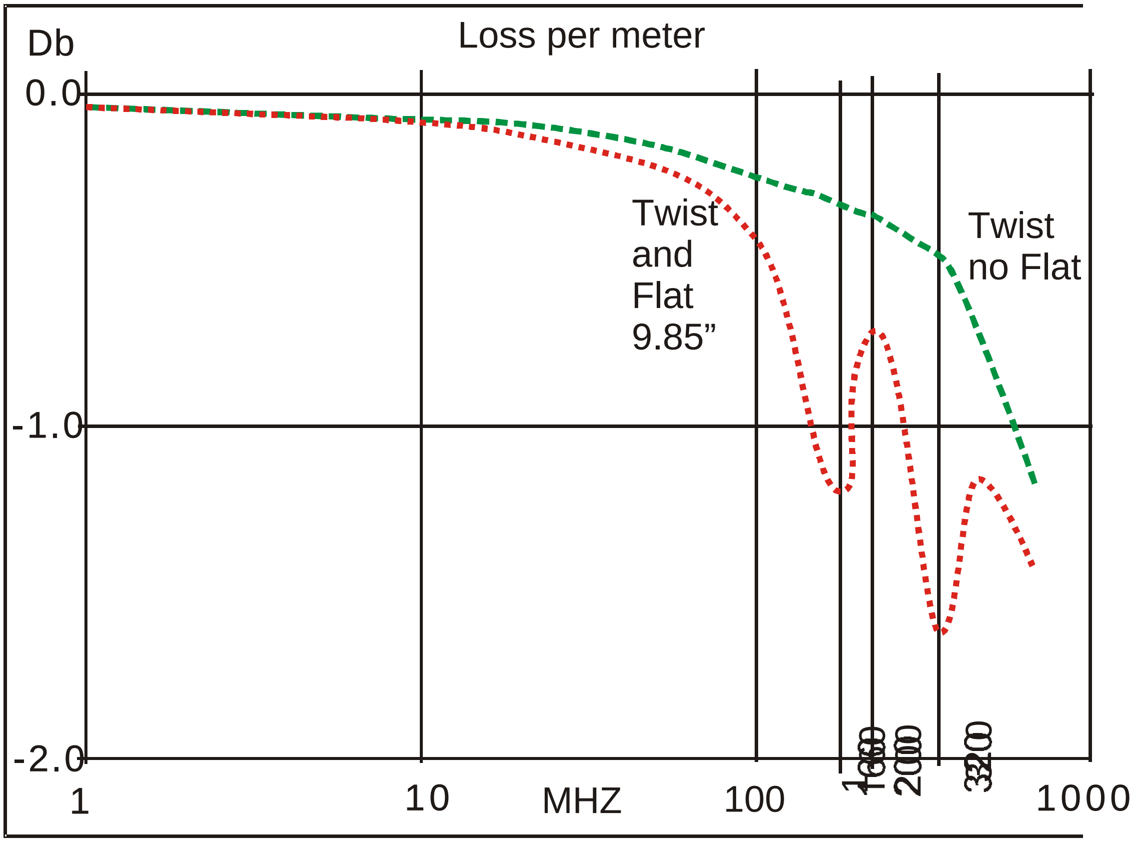

Figure 1. Twist and Flat Frequency Response

PIP Tests

PIP tests are defined with sample preparation, test fixtures, and equipment to get repeatable results in several laboratories. The PIP ad hoc group ran several round robin tests of bulk cables, cable assemblies and backplanes to ensure that the test procedures were reproducible in several laboratories. The tests of the PIP standard will produce the values needed for SCSI signal modeling (SSM) which is a technical report supporting the SCSI parallel interface standards. The SSM gives a basic confidence that the system designed will operate without periodic structure or reflection problems. SSM is based on the IBIS 3.2 modeling structure which has limited ability to model circuitry. It is based on current versus voltage (IV) structures. SSM-2 is in development and is based on IBIS X, and allows circuit models which will better simulate drivers and terminators. IBIS X is due in late 2002.

SCSI parallel interface technology is developing at a pace that doubles the performance every two years. Passive interconnect components develop at a slower pace. The PIP standard is designed to work across at least two generations of the SCSI parallel interface (SPI) standard development. Development processes are linked by the SPI requirements. Higher speeds require the ability to model the system performance to ensure that backplanes and cable assemblies will work together. The model may prove that other connectivity methods (like expanders) are required to handle the change in impedance between the cable and the backplane or an impedance transition pad.

Backplane and Cable Design and Test

Backplanes are extremely hard to design for high impedance. Often the backplane impedances with devices are much lower than the cable impedances. The effects of device loading, connectors and vias for the press pin connectors dominate the impedance calculations. Future generations of parallel SCSI will require impedance match and possible adjustable impedance terminators to reduce reflection problems. Reflections at higher speeds can be larger than the isolated bit size of signals, especially with 160 MHz in a system with FR4 or PVC. The high frequency signals can be only 30 percent of the DC signal levels.

Bulk cable traditionally has been the only thing specified in the SPI standard. The requirements have been at specific frequencies (not at swept frequencies), and cables such as twist and flat cables have not been specified. The standards have specified losses at five and 200 MHz. SPI-3 annex E was developed by the ad hoc group that is developing the PIP and SSM-2 standards. Annex E addresses only bulk cable. PIP expands the testing to include cable assemblies and backplanes.

The bulk cable must first meet all the parameters using the full bulk cable tests defined in the level one test table. The cable impedance should be tested in single ended and differential mode using a TDR test. This sends a pulse down the cable and looks at the reflected wave, which not only shows the impedance at each point of the cable, but in addition, can detect the distance from the tester at which an impedance problem occurred. The bulk cable extended impedance test is a swept frequency test from 30 to 600 MHz using a VNA. The extended impedance test will show problems with periodic structures. This is very important for twist and flat cable to insure that spacing is correct for the key SCSI frequencies; 40, 80, 160 and 320 MHz.

Single-ended and differential capacitance are measured with a level crossing rate (LCR) meter at 100KHz and 1 MHz. This is used in the SCSI signal modeling. Propagation time is measured for matching between pairs. Near-end and far-end crosstalk cannot exceed three percent at the SCSI key frequencies. Hipot, (high voltage test at very low current) tests the breakdown voltage of the insulation without degrading the insulation. Testing is done to ensure the integrity of the insulation. The dielectric constant is measured over the frequency range from 300 KHz to 600 MHz with a VNA. Each test is called out in the level one and level two test tables. There is also a section devoted to the test equipment. The test fixturing and sample length with preparation are required for each test.

Level one tests for backplanes and cable assemblies include; single-ended and differential TDR, single-ended and differential capacitance, propagation delay (difference in the pair and pair-to-pair), crosstalk (both near-end and far-end), common mode noise/crosstalk, electromagnetic interference (EMI), leakage to ground, Hipot, and DC resistance and dielectric constant over frequency.

Cable assemblies must be terminated correctly. The round cables must be cut, stripped and fanned out keeping the pairs twisted as much as possible to reduce crosstalk and impedance changes. The wires should not be re-cut. This would create different length pairs, producing skew differences between the pairs. Twist and flat cables must be designed for SPI-5 and beyond with the correct spacing to eliminate the comb filter effects at 160 MHz seen in standard twist and flat cables (see Figure 1). Twist and flat cables should be designed with the flats only where the connectors will be attached. Extra flat areas increase crosstalk and periodic structure effects.

Printed Circuit Boards, Vias and Backplanes

Printed circuit boards have several factors that must be carefully considered such as the dielectric material and thickness. Etch on the outer layers normally has 20 mils of dielectric thickness on a multiplayer FR4 board. Typically, five mil etch with five mil spacing between etch in the pair, with at least ten mil spacing to the next pair to reduce the mutual coupling, is the right impedance and spacing without the loading effects. Vias can have a dramatic effect on the impedance. SCSI devices must balance the capacitance within a pair as well as the capacitance with pair-to-pair. One feed-through with standard clearance to the power and ground plane creates a greater difference than is allowable. Enlarged clearance holes in the power and ground plane are required to reduce the capacitance of the vias.

Backplanes normally use press fit connectors, which require vias. Many backplanes have more than one power and ground plane. The capacitance to each power and ground plane can be 0.5 to one pF using standard clearance holes or three to five pF for the via without the connector or drive (add three to five pF for the connector and 10 to 15 pF for the drive). The clearance hole on each plane must be enlarged for press fit connectors. It is often better to open the entire area, and all but one ground plane under the connector on the power, to reduce the capacitance. The unloaded impedance of the backplane must be greater than 100 ohms. When the drives are added the impedance should not drop below 85 ohms differential. The distance between devices is very close— often one-inch drives are used. Etch routing should go to every other drive to add distance between the loads in order to improve the bus impedance. Drives for Ultra160 and Ultra320 SCSI are between 10 and 15 pF, then add the backplane connector and vias for the press pin connector. This can be 20 pF for each device. Prior to Ultra160 SCSI devices, 25 to 35 pF was a typical load.

Backplane spacing can have the same types of problems as cable assemblies if the spacing is at the distance where it forms a periodic structure. The attenuation can be much greater than expected, reducing the high frequency signals below the receiver's ability to detect them.

Impedance Issues

The key factors are impedance mismatches that will cause reflected wave that can approach the size of the high frequency attenuated signal and crosstalk. The crosstalk and reflected wave combined are normally worst at the first device in a backplane when the combination of cable and loaded backplane are connected. The impedance of the cable can be reduced to help the reflection problem within limits. If the reflection and crosstalk are too great, than an expander must be used to separate the impedance mismatch of the cable to the backplane. The expander receives, retimes and retransmits the signal. This allows a point-to-point connection of up to 25 meters to the backplane that can be heavily loaded. Empirical data from large configurations show the attenuation of the high frequency Ultra640 SCSI signals (single bit) that are 30 percent of the DC signal swing. These systems had periodic structures that cause the high frequency attenuation to work at Ultra640 SCSI speeds. The system must either be designed without the periodic structures or segmented by use of expanders. Even with the use of expanders the backplane may still have to be redesigned to eliminate the periodic structures at key frequencies.

Bus Configurations Explained

Figure 2 illustrates the different bus configurations.

- The top illustration is an in-the-box configuration with twist and flat cable only where there are no flats between the host bus adapter and the first drive.

- The next illustration shows an in- or outside-the-box cable to backplane configuration. If twist and flat cable is used, only the ends of the cable have flat sections. Note that outside the box, round, shielded cable would be used.

- The third illustration shows the expander on the backplane, which avoids the difference in impedance between the backplane and the cable. This allows cables to be used in a point-to-point configuration of up to 25 meters.

- The last illustration shows the backplane as a closed system that can use the programmable terminators. The programmable terminators can be adjusted to match the impedance of the backplane, reducing the terminator reflections.

Terminators before SPI-5 are specified at 105 ohms +/- five ohms. A backplane normally starts with high impedance, then as drives are added the impedance drops. The drive stub load becomes the dominant capacitance of the backplane impedance. An unloaded backplane can begin at 120 ohms differential impedance and become a loaded impedance of 50 ohms with the drive installed. The reflection from the 105-ohm terminator is as large as the Ultra640 SCSI high frequency signal. Adjusting the impedance to match the loaded backplane reduces the reflection to a small percentage of the original size of the signal.

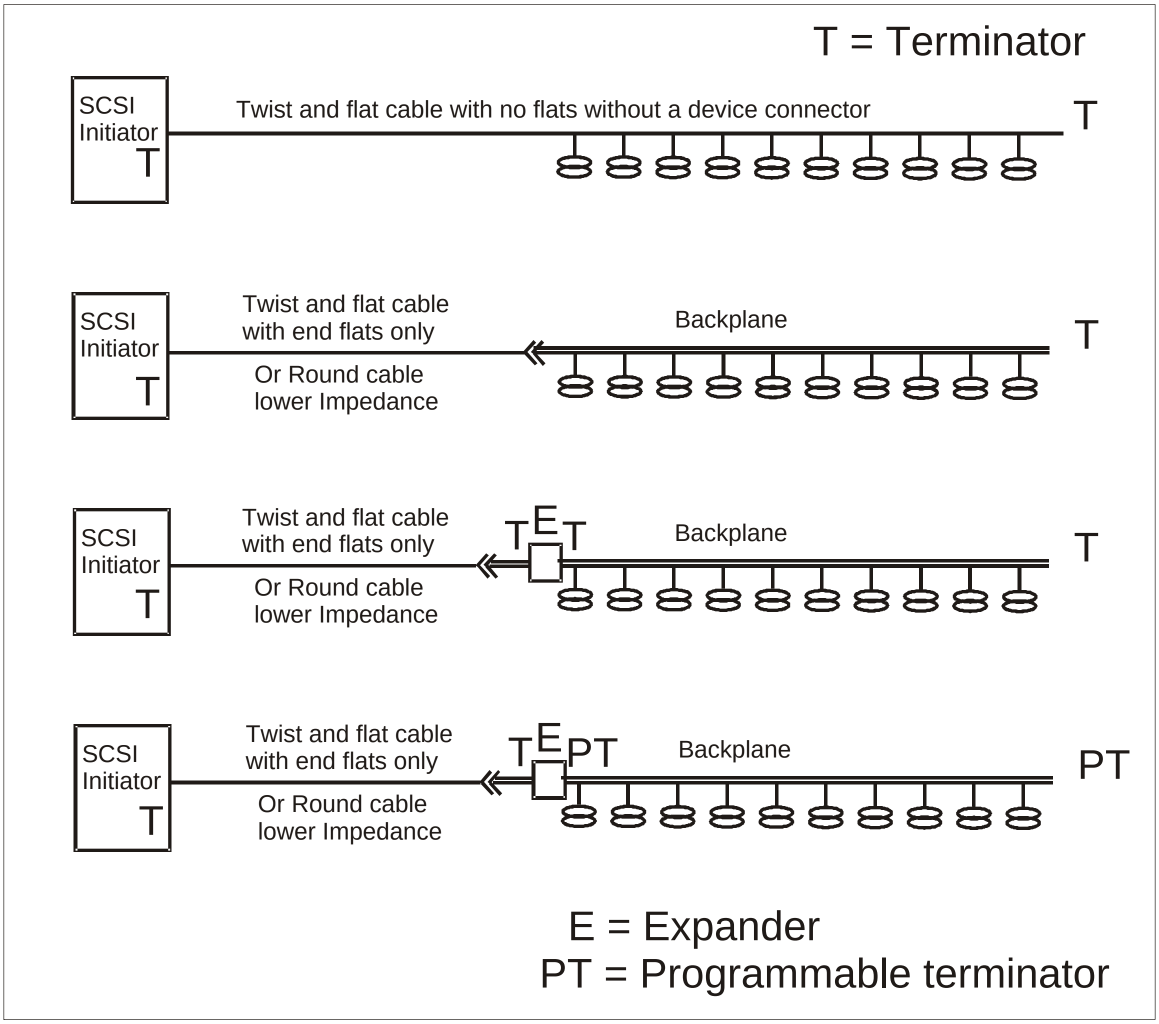

Figure 2. SCSI Bus Configurations

System Skew

Total system skew cannot be ignored. The skew is not only from the difference in wire or etch length but also from the difference in capacitance. Stubs appear as capacitance loading on the bus. Differences in the stubs on the drives will factor into the skew. The total skew budget cannot be taken from the cable and backplane only, as 50 percent of the budget can be taken by the drives.

Common mode noise and EMI come from imbalance in the system. If a differential system is carefully balanced it will not radiate and will not be susceptible to system noise. Tolerance of the etching process, capacitance to other signals or components and differences in components between the signals in a pair, can cause imbalance. Changes in the routing can compensate for component skew issues such as component package differences between signals in a pair. Component vendors need to pay a lot of attention to the choice of pins in a pair or ball grid array (BGA) substrate design and the selection of balls in the pair. Corner pins on a field programmable gate array (FPGA) can have twice the capacitance of a pin in the center of the package. Silicon capacitance has been reduced to a level so that the package capacitance becomes the dominant factor.

Trouble Shooting

There is a second level of testing defined for trouble shooting problems, which includes; eye patterns, attenuation (within the pair and pair-to-pair), rise time degradation, attenuation to crosstalk ratio (ACR) and VNA. The ACR over frequency shows the margin for the system. With higher frequencies the margin is drastically reduced because the signal is reduced with frequency and the crosstalk increases with frequency.

Twist and flat cables and backplanes require a lot of work. The reduction of crosstalk is very important. Reducing the flat area on the twist and flat cables and increasing the spacing between pairs on printed circuit boards is required to reduce crosstalk. A ground run between signal pairs will reduce the coupling between the pairs. Attenuation reduction with frequency normally means changing the dielectric.

Second level testing allows for the debug of a full system to correct cabling and backplane problems. Eye pattern tests have been key in making systems work, but as speeds increase, the analysis of the eye is more important. Knowledge of the receiver hysteresis is key in eliminating traces that the receiver would not have switched the receiver. The eye disappears with reflections and ISI issues. With receiver technology like the adaptive active filter (AAF), it is possible to not have an eye and have the system work fine. It may be necessary to view eye diagrams through a circuit that emulates the worst case AAF receiver. The swept frequency ACR test becomes the most important in understanding the system. When crosstalk approaches the high frequency signal level, even a high performance AAF receiver will not work.

Summary

SCSI is leading the way in multidrop bus performance through careful specification and test methods. Standards like PIP and SSM are requirements in high performance bus technology. SCSI technology builds on its past and is showing the way to the future. The designs of cables and backplanes must consider the future speeds to avoid problem designs at the key frequencies. Labeling of cables may be required to show that they are compatible for future generations of SCSI.

Glossary of terms used in this paper

AAF – Adaptive active filter – SCSI SPI-4 receiver option.
ACR – Attenuation to crosstalk ratio.
FEP – Flourinated ethylene propylene insulation – better frequency response than PVC.
FR4 – Standard fiberglass printed circuit board.
HDPE – Foamed polypropylene insulation – better frequency response than PVC.
Hipot - High voltage test at very low current – tests the breakdown voltage of the insulation without degrading the insulation.
PVC – Polyvinyl chloride.
TDR – Time domain reflectometer.
TPE – Thermoplastic elastomer – insulation with better frequency response than PVC.
TPO _ Thermal plastic olefin – insulation with better frequency response than PVC.
VNA – Vector network analyzer.