

Balanced LVD SCSI Drivers and Receivers

A White Paper Prepared by The SCSI Trade Association

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BALANCED LVD SCSI DRIVERS AND RECEIVERS

The requirements for LVD drivers and receivers are defined in Annex A of the SCSI Parallel Interconnect-2 (SPI-2) specification and is available at <ftp://www.symbios.com/pub/standards/io/x3t10/drafts/spi2>.

The purpose of this article is to review these requirements and to show how a balanced LVD driver provides more system margin – and reliability -- for the system designer, system integrator, or VAR.

Introduction:

Low Voltage Differential (LVD) signaling technology will be used in the next generation of parallel SCSI products. This is because the Ultra2 SCSI standard shifts the physical interface from a single-ended physical interface to an LVD physical interface. In an LVD physical interface, each signal has a dedicated return conductor as compared to a single-ended interface. An LVD driver generates this differential signaling where each SCSI signal has a plus signal (+) on one conductor and its exact complement minus signal (-) on the other conductor. LVD signaling is inherently less noisy than single-ended signaling and offers many I/O system benefits including greater cable distances, more device connectivity, and faster data transfer rates.

As the complexity and speed of I/O systems increase, design architects are typically concerned about system margin. These systems require that the designer consider electrical issues such as signal integrity, cross-talk, and ground bounce. The designer needs to understand the interface characteristics of the system such as reflections, cross talk, noise, capacitive loading, signal skew, stub lengths on transmission lines, terminator tolerances, cable impedance, etc.

To ensure that the system designer has sufficient system margin, the SPI-2 specification has defined the requirements for LVD drivers and receivers in a properly designed LVD system.

SPI-2 LVD Driver Requirement

The SPI-2 specification requires that LVD drivers have asymmetrical outputs to generate balanced differential voltages.

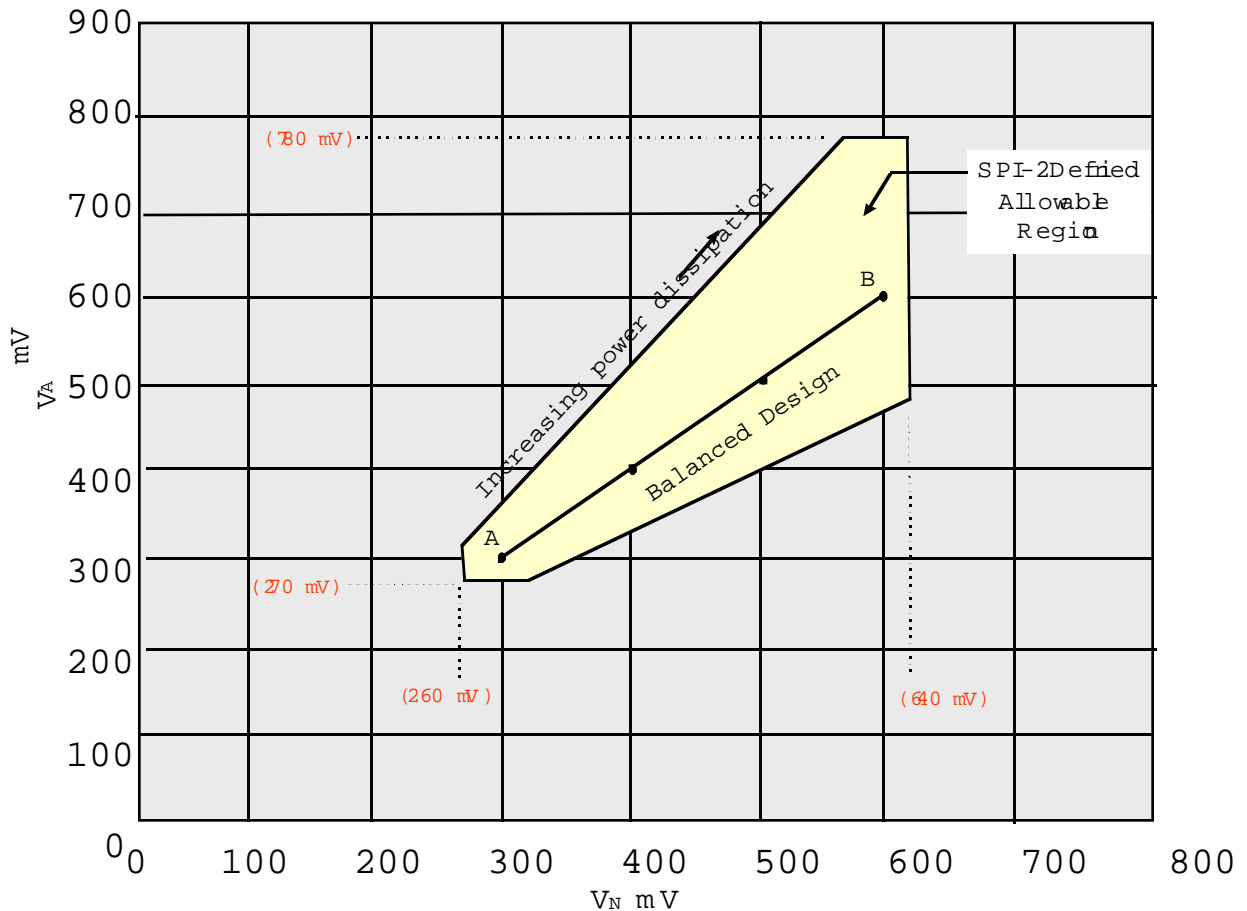


Figure 1: Domain for LVD Driver Assertion and Negation Differential Voltages

To meet this requirement, SPI-2 has defined the allowable regions, shown in Figure 1, for compliant LVD drivers and receivers. The chart shows the differential output voltage of an LVD driver when it is asserting a signal (V_A) and when it is negating a signal (V_N) on the LVD bus. (Actual measurements are determined by a differential steady-state output voltage test circuit defined in Annex A). For an asserted state, the differential output magnitude must be greater than or equal to 270 mV and less than or equal to 780 mV. For the negated state, the differential voltage magnitude must be greater than or equal to 260 mV and less than or equal to 640 mV. These allowed ranges ensure system margin by accounting for system tolerances such as variations in terminator impedance, terminator bias, cable impedance, driver current tolerances, LVD driver manufacturing tolerances, ground offsets, variations in voltage, and temperature. The requirement for V_A to be greater than 270 mV and for V_N to be greater than 260 mV is to avoid noise and cross talk problems in the LVD driver design. The chart also shows that power dissipation increases as V_A and V_N increase.

The design of a compliant LVD driver will result in an assertion signal (V_A) and negation signal (V_N) within the SPI-2 allowed region above. However, in order to maximize the greatest system margin and benefit of LVD, it is desirable to achieve a “balanced” LVD driver design. A balanced LVD driver has an assertion and negation signal the line intersecting the points A and B in Figure 1.

Balanced LVD Driver:

A balanced LVD driver results in equal differential amplitudes of the asserted state and negated state. Having a good LVD driver design provides greater system margin thus providing the designer with greater reliability and higher system integrity – a fundamental requirement in today’s server and workstation architectures.

A balanced LVD driver is desirable because it is better able to reduce cross talk, manage system skew and lower power dissipation than an unbalanced LVD driver. It has the same voltage swing in the asserted V_A state as negated state V_N that allows the LVD driver to achieve Ultra2 transfer rates while using minimal power. It will also have an equal propagation delay from input high to input low and equal rise and fall times of the differential outputs. If the delay on the input high to input low is not equal, a distorted signal occurs. Excessive over and under shoot can cause EMI or false logic state changes.

Asymmetrical outputs

The design of a balanced LVD driver requires an asymmetrical output current to generate balanced differential voltages. The SPI-2 document allows either voltage or current mode drivers.

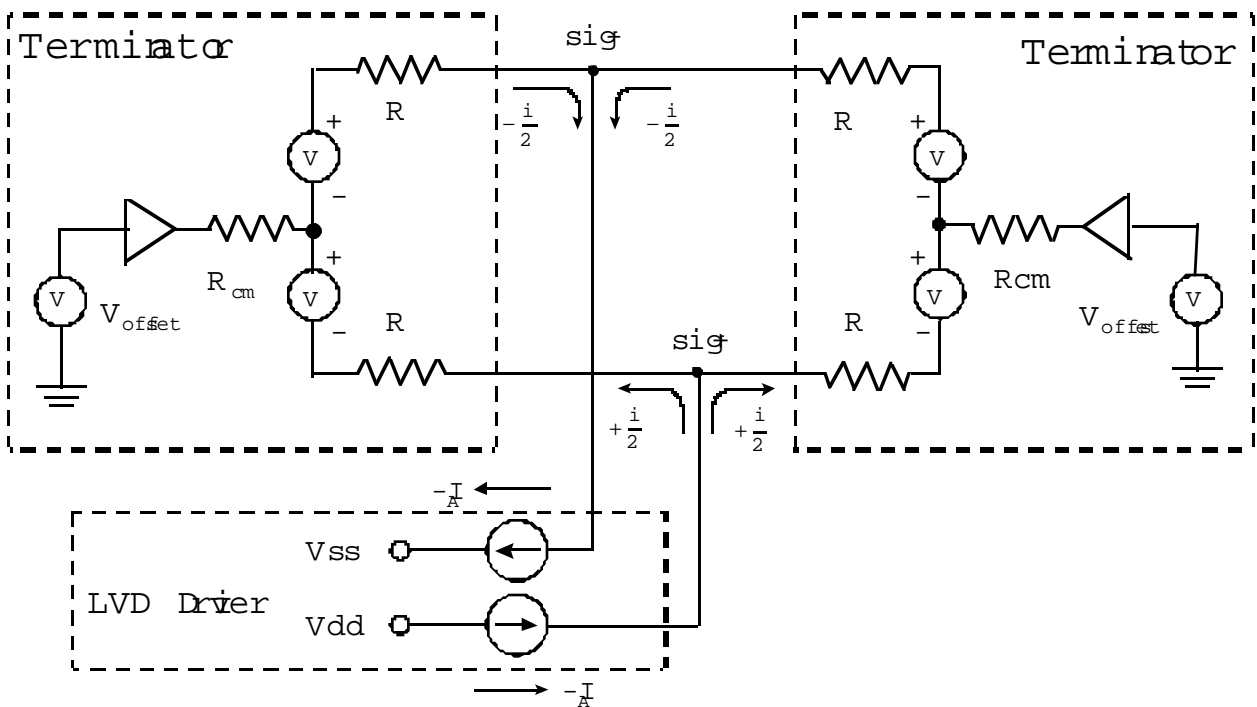


Figure 2. Asserted LVD Driver

Figure 2 shows a current mode LVD driver implementation in a terminated system. In this example, the LVD driver is asserting a signal. The terminator circuits are modeled from the system level parameters found in Annex A where V is the terminator bias voltage and R is the terminator impedance. The terminators provide the voltage source to bias the LVD bus to a logically false. This is required because the SCSI protocol requires the bus to appear logically false when it is idle.

The key to understanding the LVD bus is to recognize that the current being sourced (pushed) into one half of the differential pair is equal and opposite to the current being sunk (pulled) out of the other. The design of a balanced LVD driver requires the signal current in one conductor to be equal to the return current in the other. A balanced source means that the changes in the signal (+) current are equal to the changes in the signal (-) current.

The key to a balanced interface is a well designed differential driver. The LVD driver works to either assert a signal or negate a signal on the LVD bus. It is asserting a signal when it pushes current (i_A) to the signal (+) and pulls current from signal (-). It is negating a signal when it pulls current (i_D) to the signal (+) and pushes current from signal (-).

Performing current loop analysis on Figure A shows that the asserted current is pushed into the signal (+) and pulled from signal (-). In a perfectly balanced system, half this current would flow through the right-hand terminator, and half would flow in the left hand terminator. Following it out from the SCSI chip, into the signal (+) where it splits in half, causes a voltage drop across the bottom right resistor, flows through both right-side voltage sources, through the upper right resistor, out signal (-) back to the SCSI chip. The voltage on the Signal (-) is $V_{offset} + V - R \cdot i_A / 2$.

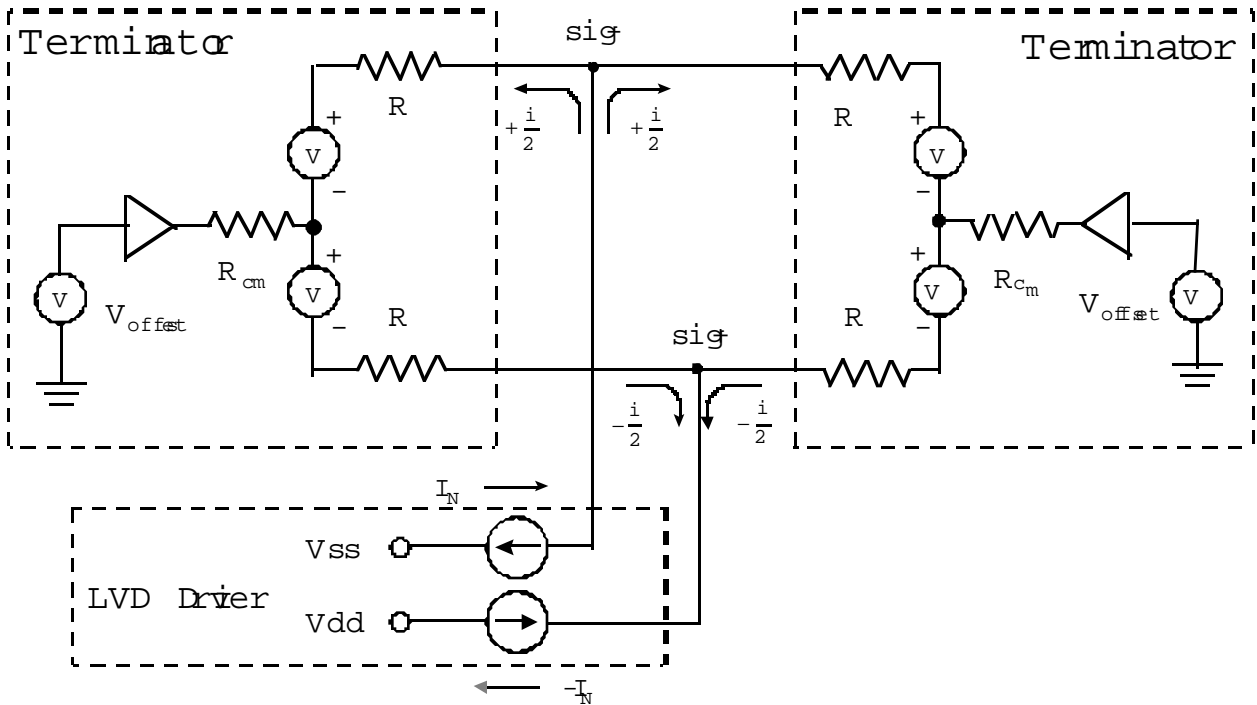


Figure 3. Negated LVD Driver

For the negated state, the current flowing into the signal (+) is pulled while the current in signal (-) is pushed. The current coming from the SCSI chip into signal (-) splits in half through the top right resistor, against both voltage sources, through the bottom right resistor, out signal (+) back to the SCSI chip. The voltage on Signal (+) is $V_{offset} - V - R \cdot i_D / 2$. A balanced design results in equal differential amplitudes of the asserted state and negated state. Setting the voltage on Signal (+) equal to the voltage on Signal (-) yields $i_A = 4V/R + i_D$. The analysis shows that the magnitude of the assertion current is different than the magnitude of the negation current. This asymmetry in output current based upon the equation above generates symmetrical differential voltages.

The test circuit defined in Annex A measures the steady-state magnitude of the differential output voltage, V_s , for the asserted state (V_A) and the negated state (V_N). A balanced LVD driver with asymmetrical outputs will result in the asserted state output voltage (V_A) being equal to the negated state output voltage (V_N).

Conclusion:

To ensure that the system designer has sufficient system margin, the SCSI Parallel Interconnect-2 (SPI-2) document has defined the requirements for LVD drivers and receivers to ensure a properly designed LVD system. The design of a compliant LVD driver will result in an assertion signal (V_A) and negation signal (V_N) within the SPI-2 allowed region. However, in order to maximize the

greatest system margin and benefit of LVD, it is desirable to achieve a “balanced” LVD driver design. A balanced LVD driver has an assertion and negation signal equal in magnitude and opposite in direction. Balanced LVD Drivers reduce simultaneous switching current, reduce ground bounce, and provide superior noise margin through common-mode noise rejection.

Acknowledgements

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Additional Information

The SCSI Trade Association has a wide variety of documents and information on SCSI Parallel Interface Technology, including presentations, articles in periodicals, seminar material and white papers. Please contact Association offices at:

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